Effect of Channel Width Variability on the Electrical Characteristics of SOI Triple Gate Junctionless Transistors

Victor Nogueira Cirillo[1], Rodrigo Trevisoli Doria[1], Member, IEEE

Centro Universitário da FEI: Electrical Egineering Department – São Bernardo do Campo, Brazil
e-mail: unievcirillo@fei.edu.br

***Abstract*—In this work, the effects of the variability of the fin width (W) on the electrical characteristics of SOI triple gate junctionless transistors were studied through three-dimensional numerical simulations. The study was performed through the simulation of the ID x VG characteristics of devices with channel lengths of 20 and 100 nm and fin widths of 9, 10, and 11 nm. Several electrical parameters have been evaluated such as the threshold voltage, body factor, subthreshold slope and the DIBL. It has been shown that the width variability is associated mainly to the threshold voltage variation for longer devices whereas in shorter ones, the body factor and the DIBL start to play an important role.**

Keywords—MOS transistors, SOI technology, junctionless transistors, variability, DIBL, short channel effects.

I. Introduction

The increasing demand for scaling the microelectronic devices has followed Moore's Law since the 60's [1]. This scaling related to requirements in terms of processor speed in today's chips, can only be achieved with the devices' miniaturization [2].

Nowadays, the most used devices in microelectronics industry are transistors fabricated in metal-oxide-silicon (MOS) technology. However, the miniaturization of these devices causes the reduction of control over the depletion charges in their channel region. This adverse effect is responsible for the so-called short channel effects (SCEs), which are responsible for the degradation of several device parameters, causing reduction in threshold voltage (V_{Th}) and degradation in the subthreshold slope [3,4]. Hence, the microelectronics industry has been developing new technologies to reduce these negative effects.

One of the developed technologies is the silicon-on-insulator (SOI) devices. In this technology, a dielectric insulator layer, called buried oxide (BOX), is introduced between the active region of the silicon wafer (drain, source and channel) and the substrate. As a result, the effect of parasitic capacitances is reduced [5].

Another technology developed, frequently used combined with SOI, is the multiple gate architecture. This ensures improved electrostatic control over the depletion charges in the channel region due to the voltage being applied in different channel planes, i.e., for a triple gate transistor, one gate is placed at the top of the silicon layer and the other two at their laterals. For that reason, multiple gate devices are able to conduct more current than conventional technologies [6].

In order to reduce the channel length to values below 20 nm, the junctionless nanowire transistor (JNT) technology was developed. Differently from conventional inversion mode MOS transistors, JNTs have the drain, source and channel regions with the same doping type and concentration [6,7]. Their longitudinal section along the channel region can be visualized in Fig. 1.

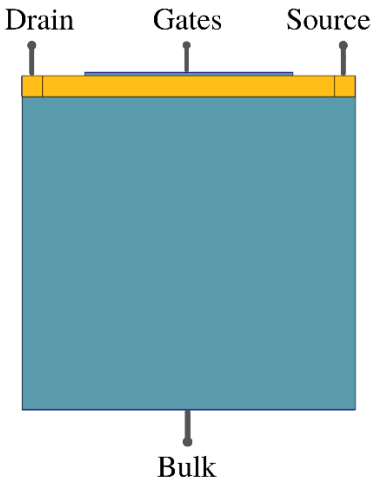

Fig. 1. Longitudinal section of the physical structure of a junctionless SOI transistor. Image taken from Sentaurus Device simulator, with the actual proportions of the simulated devices.

In contrast to conventional technologies, JNTs do not conduct through an inversion layer, but in partial depletion or accumulation regime. Their fabrication is designed to ensure that the difference between the work functions of the gate material and the silicon in the channel region is able to make the entire channel depleted while the device is at off-state. By applying a positive gate voltage (V_{GS}) at an n-type transistor, this depletion layer is reduced, and conduction starts when threshold voltage is reached. In this condition, a bulk conduction path is observed in the neutral region of the silicon layer. As V_{GS} is increased, the neutral path becomes larger and, at flatband voltage (V_{FB}), it fills the whole silicon thickness. For even larger V_{GS}, an accumulation layer is formed close to the gate to channel interface, giving rise to a second current component. Despite their advantages, these transistors are subject to significant variability of their electrical characteristics, depending on their doping concentration and dimensions [8, 9, 10, 11, 12].

Because JNTs have a different conduction mode and their electrical characteristics are very dependent on the doping variability and their dimensions, some recent works have been conducted to study the variability in JNTs [12, 13, 14, 15, 16, 17]. In [13] analyses are performed from a compact analytic model and Monte Carlo simulations on triple gated JNTs, and in [14, 15] for double gated JNTs with technology computer-aided design (TCAD) simulations. Experimental analyses about the variability based on several measurements are shown in [16, 17]. In addition, in [12], an analytical model for

the variability of the threshold voltage and drain current in JNTs is proposed.

In the current methods of fabrication of this type of device it is common to occur variations in the channel width, however, the effects of these variations in the electrical characteristics of the transistors are still not completely understood. Therefore, throughout this work, analyses will be performed around drain current (I_D), threshold voltage (V_{Th}), drain induced barrier lowering (DIBL) effect, subthreshold slope (S), body factor (n) and ΔI_D curves for devices with different fin width (W) and channel length (L) biased at different drain voltages (V_{DS}).

After this introduction, Section II presents the characteristics of the simulations performed and the models applied in simulations. Besides that, the extracted I_D x V_G curves are shown. In Section III, the analyses performed are presented in two subsections, divided into Section III.A where the sub threshold voltage is discussed and Section III.B that deals with the body factor of the devices. Finally, Section IV is dedicated to present the conclusions of this work.

II. Devices and Simulations Characteristics

The analyses were carried out from data obtained through three-dimensional numerical simulations of SOI junctionless triple gate MOSFETs, performed in the Sentaurus Device simulator [18]. In this software, the structure of the devices can be discretized in a grid of points, and finite element method is used to solve Poisson and continuity equations along the whole structure. So that, it is possible to simulate 3D structures such as the studied one.

For the simulations, n-type devices with different physical characteristics were defined. All of them present silicon layer thickness (t_{si}) of 10 nm, source-drain length (L_{fd}) of 30 nm, gate oxide thickness (t_{ox}) of 1.5 nm, buried oxide thickness (t_{box}) of 150 nm, and arsenic doping at a concentration of $1x10^{19}$ cm^{-3}. These physical characteristics are similar to the experimental ones presented in [19]. With these features as standard, the I_D x V_{GS} curves for devices with channel lengths of 20 and 100 nm and fin widths of 9, 10, and 11 nm, were simulated for different V_{DS}. Models for mobility dependence on the lateral electric field (high field saturation), band gap narrowing and carrier generation and recombination (SRH) were applied in the simulations.

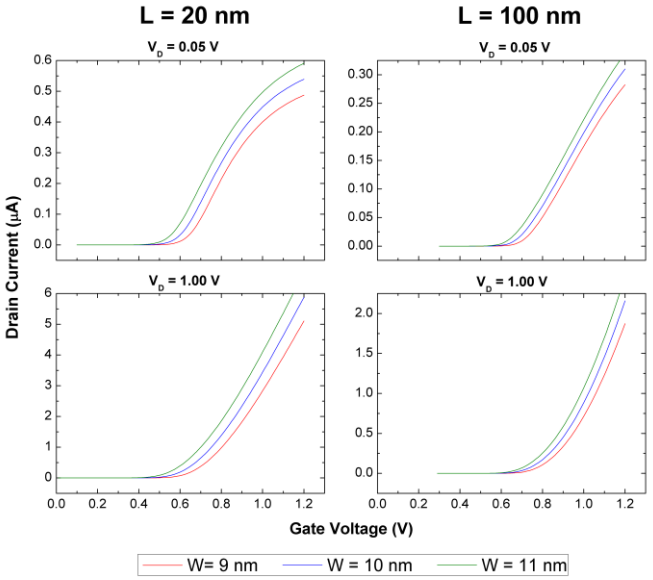

Fig. 2. I_D x V_G characteristic curves for the six simulated devices, applying 0.05 and 1.0 V between drain and source.

As mentioned, the simulations were performed by extracting the characteristic curves of the drain current (I_D) for each device. For that, a temperature of 300 K, substrate bias (V_{BS}) of 0 V and drain-source voltage of 0.05 V and 1 V were considered. Fig. 2 shows the I_D x V_G characteristic curves for devices with L = 20 nm (left graphs) and 100 nm (right graphs) and V_{DS} = 0.05 V (top graphs) and 1.0 V (bottom graphs). These curves were validated through experimental data and the results of the physical model presented in [20].

III. Variability Analyses

From the obtained curves, analyses were conducted for the threshold voltage (V_{Th}), subthreshold slope (S) and body factor (n) parameters, verifying how the slight variation of the channel width influences on these variables. Additionally, the impact of the short channel effects in the studied parameters will be highlighted.

A. *Threshold Voltage (V_{Th})*

For the extraction of the threshold voltages of the devices, the second derivative method was used. This method consists in extracting V_{Th}, obtaining it at the maximum point of the transconductance derivative, i.e., the second order derivative of the I_D x V_{GS} (d^2I_D/dV_{GS}^2). At this point, the value of V_{GS} V_{Th}. This method is used to reduce the effects of the series resistance of the devices [21].

This procedure was done for the simulated devices with low value of V_{DS}. For high values, on the other hand, the effect of the horizontal electric field affects this parameter extraction. Therefore, for high values of V_{DS}, the threshold voltage was extracted through the I_D x V_{GS} at V_{DS} = 1.0 V as the V_{GS} for which the drain current was the same as the one obtained for V_{GS} = V_{Th}, in the I_D x V_{GS} at V_{DS} = 0.05 V. Fig. 3 shows results obtained for the threshold voltage as a function of channel width for the two channel lengths (top and bottom graphs, respectively).

In Fig. 3, it is observed that the variation of the channel width affects the threshold voltage of the device. It was noted, for both channel lengths, that when increasing the channel width by 1 nm, the threshold voltage was decreased by approximately 0.04 V, having a behavior inversely proportional to W_{fin}.

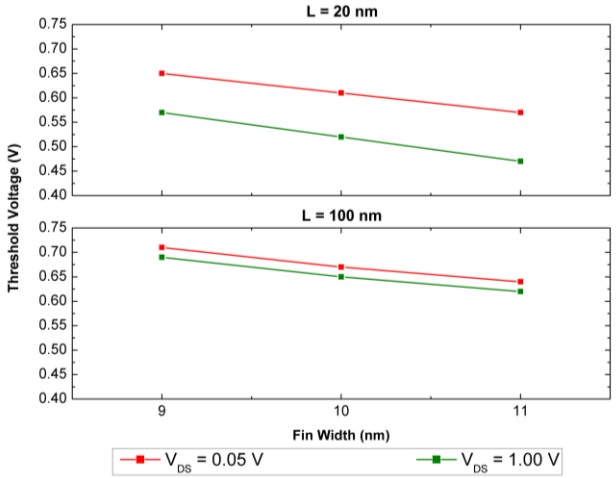

Fig. 3. Threshold voltage (V_{Th}) as a function of channel width (W_{fin}).

Furthermore, it is also seen that the increase of V_{DS} is responsible for a slight change in the slope of V_{Th} as a function of W. This phenomenon is associated with the drain induced barrier lowering (DIBL) effect, one of the short channel effects, which is related to the extension of the drain depletion region into the channel with the V_{DS} increase. The DIBL is commonly presented in mV/V and indicates the variation in threshold voltage caused by the addition of 1 V in the drain voltage. It can be obtained from (1)

$$DIBL = \frac{V_{Th\,(V_{DS}\,=\,0.05\ \mathrm{V})} - V_{Th\,(V_{DS}\,=\,1.0\ \mathrm{V})}}{(V_{DS_{\mathrm{high}}} - V_{DS_{\mathrm{low}}})} \quad (1)$$

where V_{DShigh} and V_{DSlow} correspond to the drain voltage values of 1.0 V and 0.05 V, respectively. The DIBL values obtained are shown in Fig. 4.

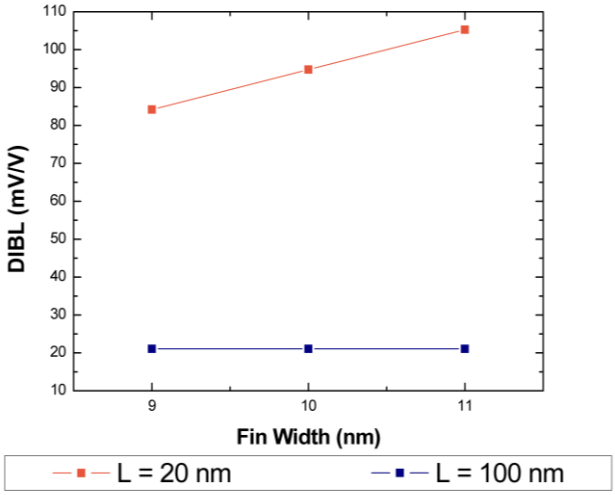

Fig. 4. Graph with the DIBL values for each device.

Observing the results, the short channel effect associated with the 20 nm channel length devices is evident in comparison to the L = 100 nm. In the former, the DIBL values are considerably higher and present a dependence with the channel width, due to the worsening of the capacitive coupling. Devices with 100 nm channel length, on the other hand, present low and constant DIBL values with width variation.

Despite the work function variability is not contemplated in this work, it is acknowledged that this parameter presents a proportional dependence with V_{Th}. Therefore, any oscillation in the work function will cause a constant variation in the threshold voltage of the devices.

B. Body factor (n)

The next step of analyses aimed to evaluate the dependence with channel width of the subthreshold slope (S) and body factor (n) of the devices. The body factor of transistors can be obtained by the ratio between the experimental subthreshold slope (S_{exp}) and its theoretical limit (S_{teo}). The latter is calculated using the values of the Boltzsmann constant (k), temperature (T) in Kelvin and the electron charge (q) as shown in (2)

$$S_{teo} = \frac{kT}{q} ln(10) \quad (2)$$

The S_{exp} values were acquired from the curve of the inverse of the log derivative of the current curve (dV_G x $d\log(I_D)$). This curve shows a plateau at its beginning, i.e., for V_{GS} lower than V_{Th}, whose values correspond to S_{exp}, given in mV/decade. Fig. 5 shows the graph obtained with the subthreshold slope and body factor values for the devices as a function of the fin width.

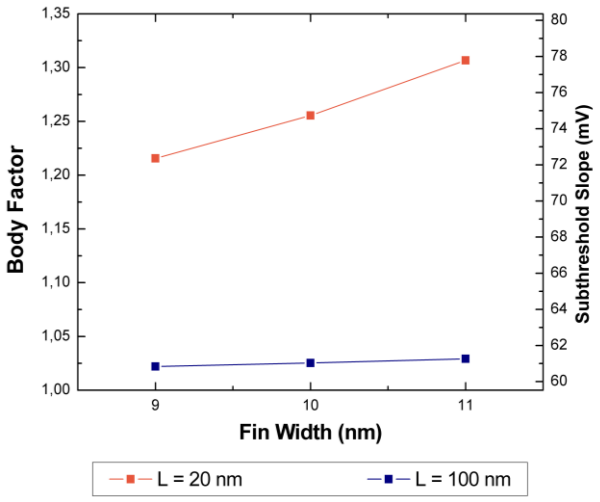

Fig. 5. Values of the body factor and subthreshold slope for the 20 and 100 nm length devices and 0.05 V drain voltage.

Analyzing the results, it is seen that, as expected, by increasing the fin width the capacitive coupling of the device is deteriorated and thereby the values of n and S are increased. However, it was noticed that this increase is more evident in the devices with short channel, and, in addition, their average values are higher, which can be attributed to the occurrence of SCEs.

In purpose of investigating the effect of the subthreshold slope on the current of the devices, the variation of the drain current (ΔI_D) was plotted as a function of V_{GS} for W changing

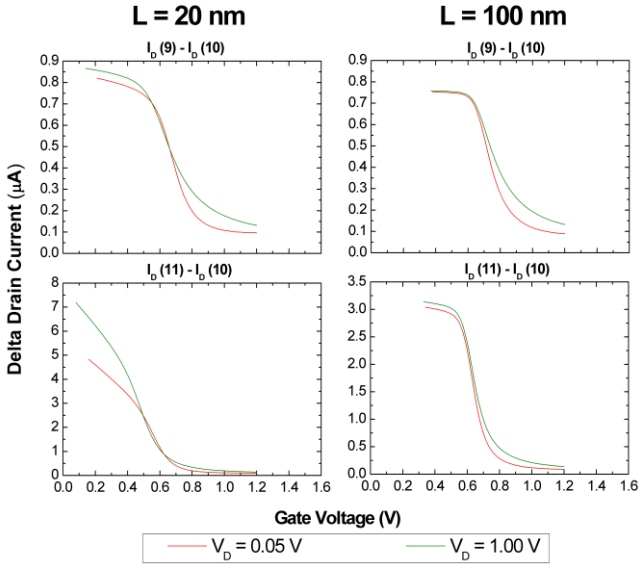

Fig. 6. ΔI_D x V_G graphics plotted for the devices.

from 9 to 11 nm. To obtain the ΔI_D x V_{GS} curves, the device with intermediate width (W = 10 nm) was considered as reference. By following these steps, the curves presented in Fig. 6 were obtained.

Examining the ΔI_D x V_G curves, it is possible to extract some important information about the operation of the devices. In its beginning, where the gate voltage is lower than the threshold voltage, it is possible to observe a plateau of the difference between the currents, where the effect of the W variation is larger. This region corresponds to the transistor switched off, conducting predominantly through diffusion mechanism. The difference between ΔI_D of the devices is explained by the different subthreshold slopes (and body factor) of the devices combined with the different threshold voltages similarly as stated in [12]. The effect of the body factor is observed mainly for devices with L = 20 nm, where ΔI_D increases for lower V_{GS}.

For $V_G > V_{Th}$, the device is switched on and starts to conduct predominantly through drift mechanism. The difference between currents drops rapidly reaching low values. In this case, the operating regime is no more associated with the subthreshold slope.

In Fig. 6, the curves for the 20 nm length devices show different slope at low V_{GS} depending on the V_{DS} value. This can be attributed to the DIBL effect. As mentioned before, this phenomenon is present in short channel devices, and leads to the variation of V_{Th} with increasing V_{DS}. This effect is more pronounced when comparing the also be observed by the displacement between the ΔI_D curves for devices of W = 11 and 10 nm, indicating the poorer capacitive coupling of the wider device.

IV. Conclusions

This paper presented an analysis, through three-dimensional numerical simulations of the electrical characteristics in SOI triple gate junctionless transistors, several important electrical parameters of these devices, such as the threshold voltage, body factor, subthreshold slope, and DIBL.

The simulated structures were chosen in order to verify the effect of varying the fin width for long and short channel devices. These devices have channel lengths of 20 and 100 nm and fin widths of 9, 10, and 11 nm. The simulations were performed using the Sentaurus Device software, and the obtained I_D x V_G curves were validated through experimental data and the results of the physical model.

Through the analyses, it was shown that the variations of the threshold voltage are mainly related to the variability of the fin width in the long channel devices, whereas for the shorter ones, the influence of the body factor and DIBL present higher representativeness. The short channel devices showed DIBL values approximately four times higher than the long ones. This justifies the increased influence of the applied drain voltage on their electrical characteristics.

Acknowledgments

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